



IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants: Liao et al.

Case: 761P7

Serial No.: 08/825,360

Filed: March 28, 1997

Group Art Unit: 2814

Examiner: Phat X. Cao

Title: INTERCONNECT STRUCTURE FOR USE IN AN INTEGRATED
CIRCUIT

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

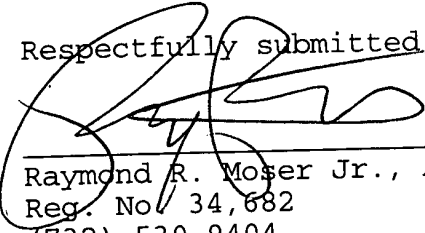
S I R:

I believe that **no additional claim fee** is required for the accompanying Response to Restriction Requirement. My belief is based upon the following calculations:

	<u>Independent</u>	<u>Total claims</u>
Claims now pending	2	33
Less: Highest number of claims previously paid for	4	53
Fee due:	<u>0</u> x \$78.00 +	<u>0</u> x \$18.00 = \$0.00
Fee for newly added multiple dependent claims		\$0.00
Reduction in claim fee due to small entity		- \$0.00
Total fee due		\$0.00

In the event I am mistaken and a fee is due, kindly charge that fee to deposit account number 20-0782. To facilitate that charge, a duplicate copy of this letter is enclosed herewith.

Respectfully submitted,


Raymond R. Moser Jr., Attorney
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2-26-99

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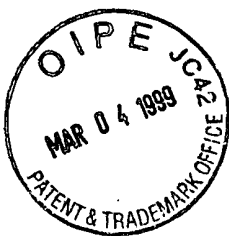
Patent Counsel
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February 26, 1999
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#7
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S I R:

Response to Restriction Requirement

In response to the office action (paper number 6) dated **January 28, 1999** which imposed a restriction requirement in the above-captioned patent application, the applicant provisionally elects to prosecute claims **21-53**, i.e., **Group II**. Nevertheless, the applicants respectfully traverse this requirement.

Claims 1-20 (Group I) are drawn to a structure in an integrated circuit and claims 21-53 (Group II) are drawn to a method for making a structure in an integrated circuit. Claim 21 recites "[a] method for forming a structure in an integrated circuit, said structure extending from a conductive surface through a channel having inner walls extending above said conductive surface said method including

the steps of: (a) depositing a layer of a refractory metal on said conductive surface and said inner walls of said channel; and (b) forming a layer of a metal nitride on said layer of said refractory metal, wherein said layer of said metal nitride has a thickness extending from said layer of said refractory metal of less than 130 Å."

The Examiner states that the related inventions I and II are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different products or (2) that the product as claimed can be made by another and materially different process (MPEP §806.05(f)). The Examiner gives an example of a method to form the recited structure by forming a temporary mask having a desired channel upon a disposable non-semiconductor substrate, depositing a layer of metal nitride over the temporary mask, forming a refractory metal on the layer of metal nitride, depositing a conductive layer on the layer of refractory metal, and finally, removing the disposable substrate and the temporary mask. The Examiner states that this method would not require a step of forming a layer of a refractory metal before a layer of a metal nitride, thus implying that the recited structure can be formed by this materially distinct process. The applicants respectfully disagree.

Claims 1 and 21 are drawn respectively to a structure and a method of forming a structure in an integrated circuit. As such, it is implicitly understood that the structure be formed upon a semiconductor substrate, either directly or indirectly upon other intermediate material layers. It is well known that forming an integrated circuit requires process sequences whose general approach is well developed, after much experimentation, and known to those skilled in the art. Typically, a semiconductor substrate, e.g., single

crystal silicon, is used as a starting material, and device structures are formed upon this substrate by depositing or growing material layers under controlled conditions. The method proposed by the Examiner cannot realistically be used to form such a structure as part of an integrated circuit.

Instead, the Examiner's method forms either a free-standing structure (after the removal of the mask/substrate), or a "reverse tone" structure resting upon the temporary mask/substrate. To arrive at a structure in an integrated circuit, a semiconductor substrate has to be formed somehow upon this reverse tone structure. The applicants respectfully submit that such a technology does not currently exist - e.g., forming single crystal silicon requires crystallization at a highly controlled purity and temperature environment, which is incompatible with the presence of the metal nitride/metal structure. Even if one can somehow place a semiconductor material upon this reverse tone structure, the applicants are not aware of any existing techniques which would allow the integration of the structure and the semiconductor material into an integrated circuit. Thus, the method proposed by the Examiner cannot be used to form a structure in an integrated circuit, as recited in claims 1 and 21. As such, the applicants submit that the process of claim 21 is not capable of producing other materially different products that are different from those in claims 1-20, and the product cannot be made by another materially different process than that recited in claims 21-53. Therefore, the applicants respectfully request a reconsideration and withdrawal of the restriction requirement.

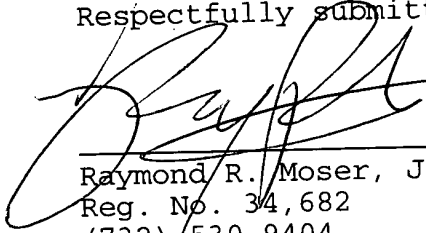
To the extent this restriction requirement is maintained by the Examiner, the applicants reserve the right to subsequently file divisional applications in order to



prosecute the inventions recited in any one or more of the non-elected groups of claims.

Respectfully submitted,

2-26-99


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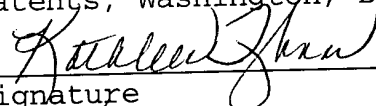
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Kathleen Faughnan
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